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**SI2302 SOT-23-3**

N-Channel Enhancement Mode Power MOSFET

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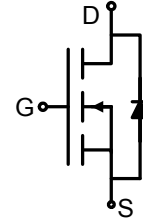


**SOT-23 Plastic-Encapsulate MOSFETS**

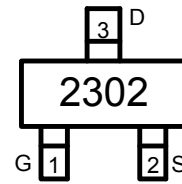
**SI2302 N-Channel Enhancement Mode Power MOSFET**

**Description**

The SI2302 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



Schematic diagram



Marking and pin assignment



SOT-23 top view

**General Features**

- $V_{DS} = 20V, I_D = 4A$   
 $R_{DS(ON)} < 59m\Omega @ V_{GS}=2.5V$   
 $R_{DS(ON)} < 45m\Omega @ V_{GS}=4.5V$
- High power and current handling capability
- Lead free product is acquired
- Surface mount package

**Application**

- Battery protection
- Load switch
- Power management

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
2302	SI2302	SOT-23	Ø180mm	8 mm	3000 units

**Absolute Maximum Ratings ( $T_A=25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	4	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	10	A
Maximum Power Dissipation	$P_D$	1	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	125	$^\circ C/W$
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**Electrical Characteristics ( $T_A=25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	20	22	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=20V, V_{GS}=0V$	-	-	1	$\mu A$

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <small>(Note 3)</small>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.85	1.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=2.5V, I_D=2.5A$	-	37	59	m $\Omega$
		$V_{GS}=4.5V, I_D=2.9A$	-	30	45	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=2.9A$	-	8	-	S
<b>Dynamic Characteristics</b> <small>(Note 4)</small>						
Input Capacitance	$C_{iss}$	$V_{DS}=10V, V_{GS}=0V,$ $F=1.0MHz$	-	300	-	PF
Output Capacitance	$C_{oss}$		-	120	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	80	-	PF
<b>Switching Characteristics</b> <small>(Note 4)</small>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=2.9A$ $V_{GS}=4.5V, R_{GEN}=6\Omega$	-	10	15	nS
Turn-on Rise Time	$t_r$		-	50	85	nS
Turn-Off Delay Time	$t_{d(off)}$		-	17	45	nS
Turn-Off Fall Time	$t_f$		-	10	20	nS
Total Gate Charge	$Q_g$	$V_{DS}=10V, I_D=2.9A,$ $V_{GS}=4.5V$	-	4.0	10	nC
Gate-Source Charge	$Q_{gs}$		-	0.65	-	nC
Gate-Drain Charge	$Q_{gd}$		-	1.2	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <small>(Note 3)</small>	$V_{SD}$	$V_{GS}=0V, I_S=2.9A$	-	0.75	1.2	V
Diode Forward Current <small>(Note 2)</small>	$I_S$		-	-	4	A

## Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

## Typical Electrical and Thermal Characteristics

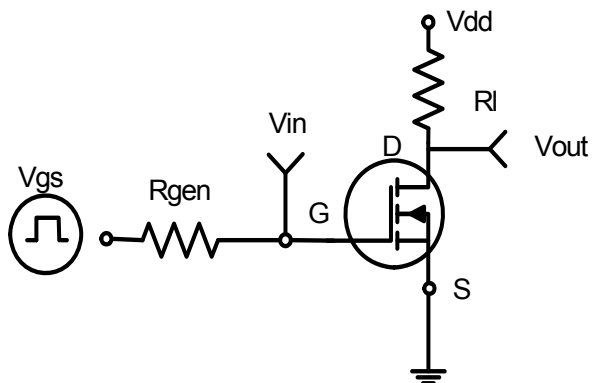


Figure 1: Switching Test Circuit

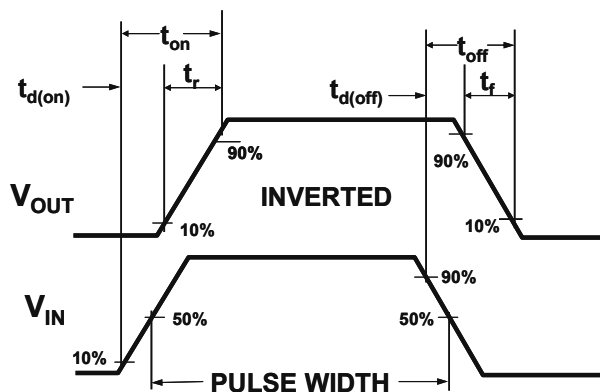


Figure 2: Switching Waveforms

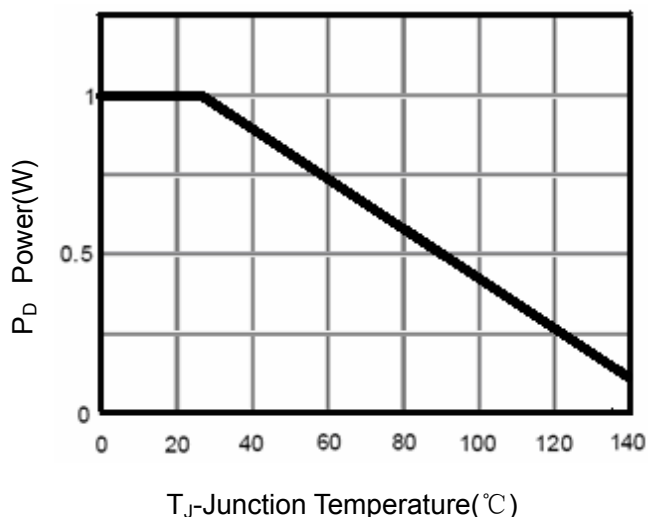


Figure 3 Power Dissipation

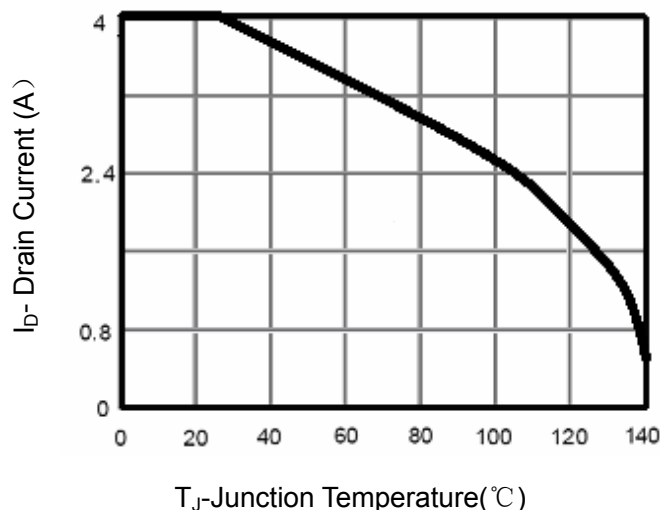


Figure 4 Drain Current

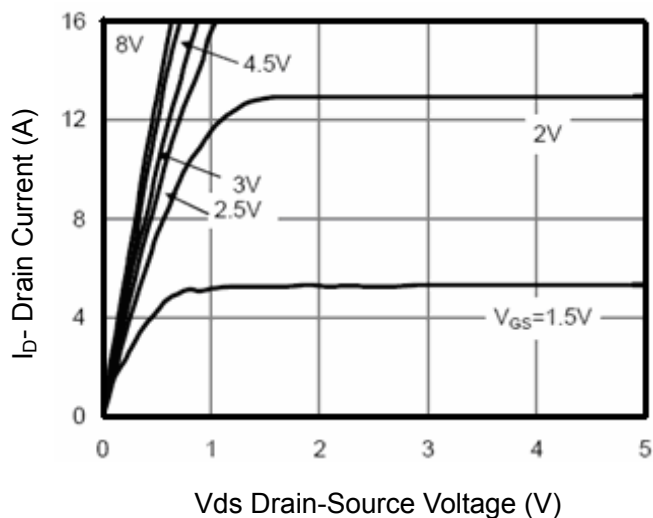


Figure 5 Output Characteristics

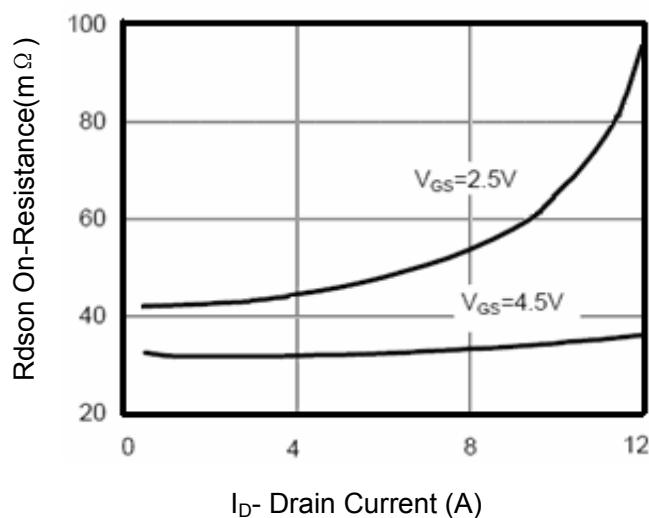
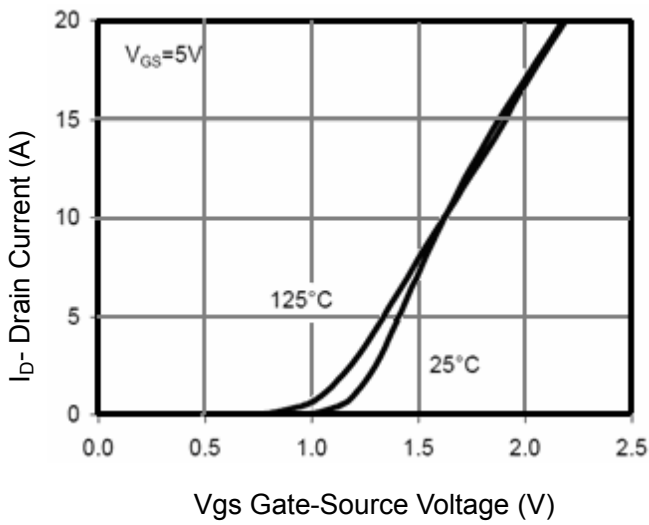
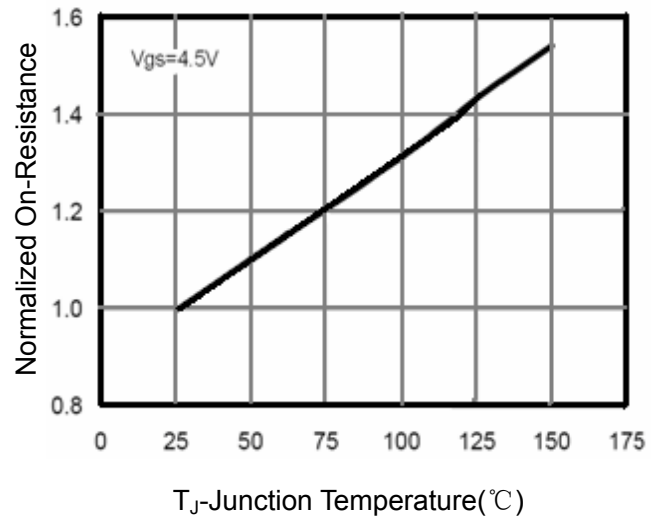


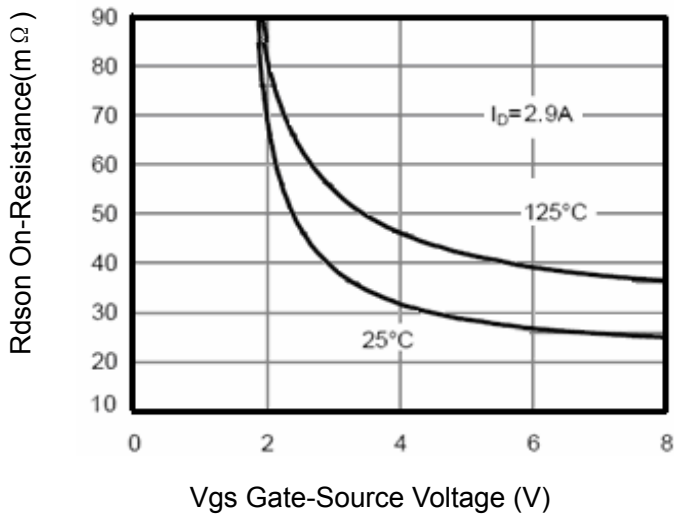
Figure 6 Drain-Source On-Resistance



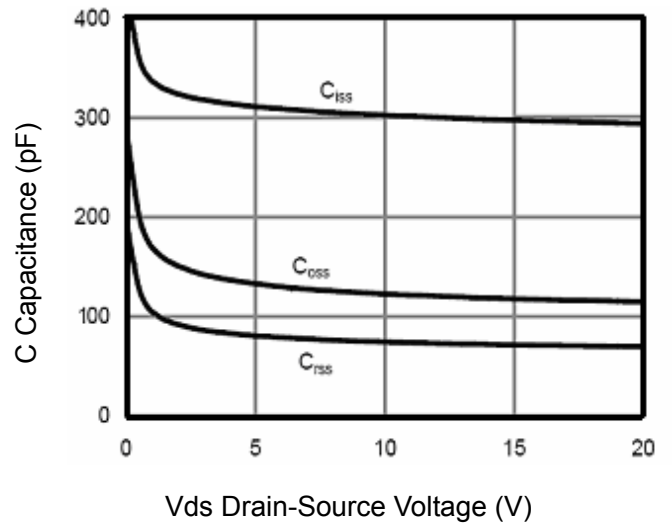
Vgs Gate-Source Voltage (V)  
**Figure 7 Transfer Characteristics**



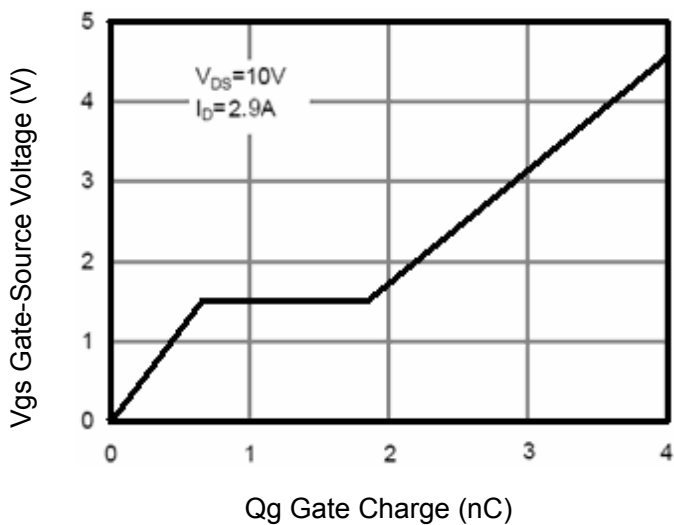
$T_J$ -Junction Temperature(°C)  
**Figure 8 Drain-Source On-Resistance**



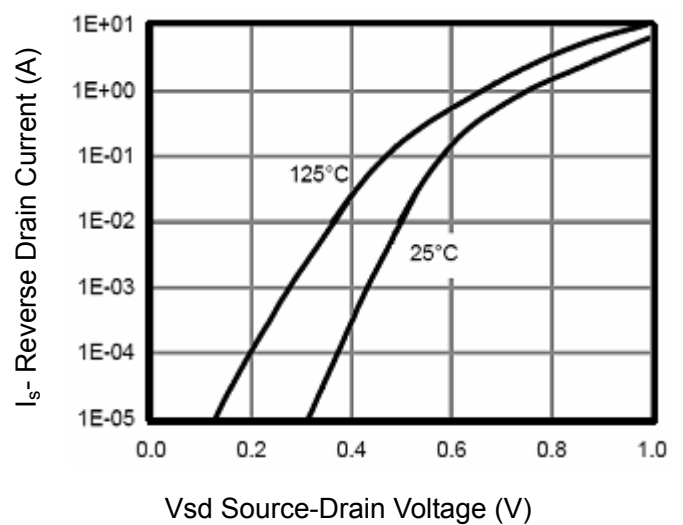
Vgs Gate-Source Voltage (V)  
**Figure 9 Rdson vs Vgs**



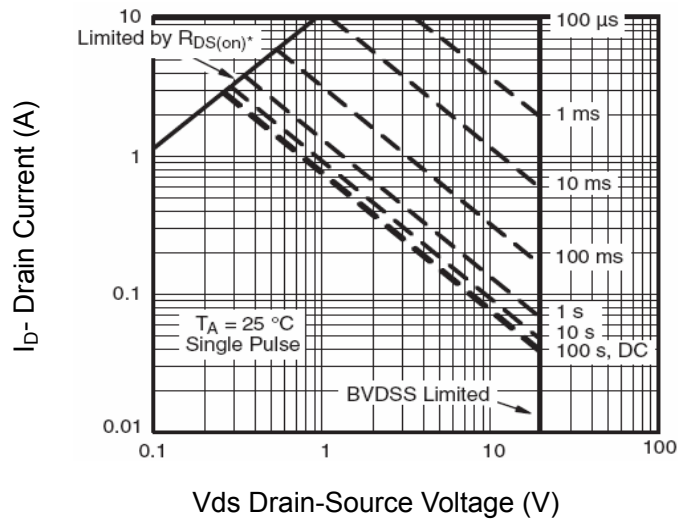
Vds Drain-Source Voltage (V)  
**Figure 10 Capacitance vs Vds**



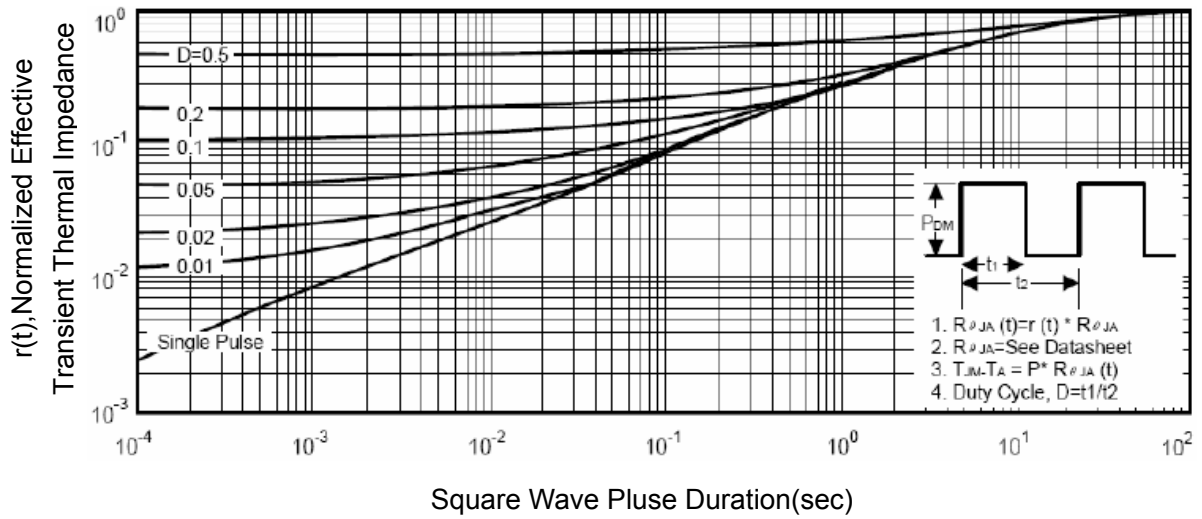
Qg Gate Charge (nC)  
**Figure 11 Gate Charge**



Vsd Source-Drain Voltage (V)  
**Figure 12 Source- Drain Diode Forward**



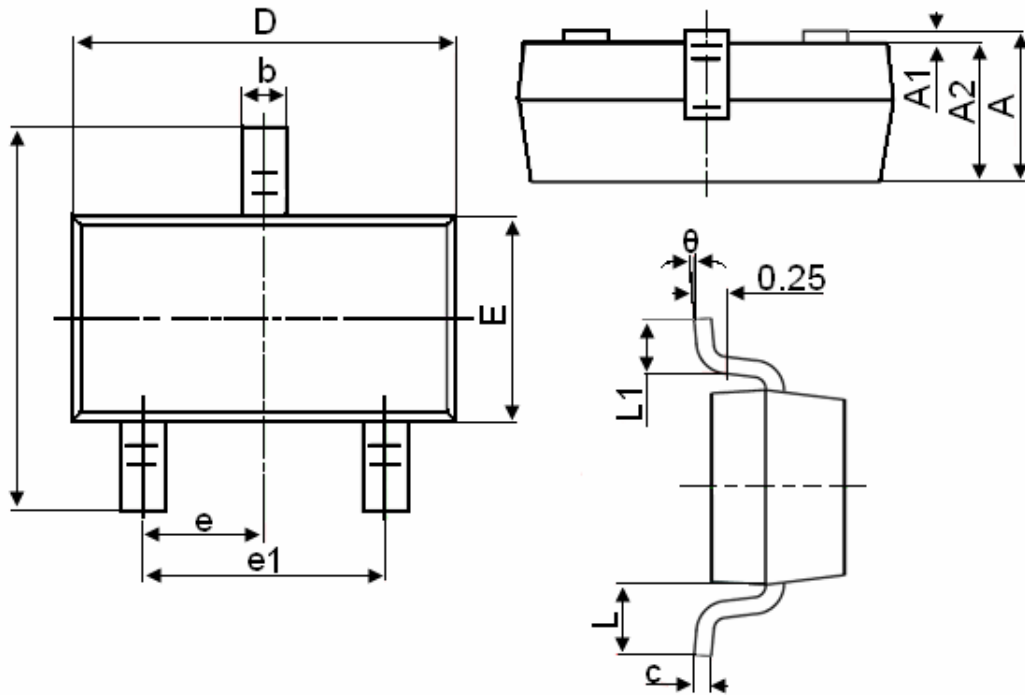
**Figure 13 Safe Operation Area**



**Figure 14 Normalized Maximum Transient Thermal Impedance**

# SI2302

## SOT-23 Package Information



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
$\theta$	0°	8°

### Notes

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.